REMARKS

Claims 1 and 12 to 15 have been amended and claims 2, 8, 9 and 13 have been indicated to be allowable. Claims 1 to 12, 14 to 16 and 18 remain active in this application and claim 17 has been withdrawn from consideration

Table 1 on page 19 of the application as filed has been transferred to page 9, between lines 18 and 19.

Claims 16 and 18 were rejected under 35 U.S.C. 112, first paragraph, as filing to comply with the written description requirement. The rejection is respectfully traversed.

The "low dielectric constant sheath surrounding each wire, said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads" is clearly shown in Fig. 4a. The specification also states at page 10, lines 20ff that "[t]he coating, or sheath 45 which has been applied after the wire bonding process, extends onto both the chip surface and the portion of the lead where the wire is attached. The use of the term "substantially" does not render the claim indefinite since this term is used to cover the case wherein some other insignificant portion of the chip may be covered by the sheath.

Claims 14 and 15 were rejected under 35 U.S.C. 112, second paragraph as being indefinite. These claims have been amended to overcome the rejection.

Claim 1 was rejected under 35 U.S.C. 102(a) as being anticipated by Applicants' Admitted Prior Art (AAPA). The rejection is respectfully traversed.

Claim 1 requires, in addition to other features, a relatively low dielectric constant sheath surrounding each wire. AAPA does not show a sheath surrounding the wire and clearly does not show a low dielectric constant sheath.

Claim 1 further requires a mold compound encasing the chip, sheathed wires, and leads having a dielectric constant higher than the dielectric constant of said dielectric sheath. Clearly, no such structure is shown by AAPA in combination with the relatively lower dielectric constant sheath.

Claims 3 to 7 were rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art. Since no specific patents are mentioned, it is assumed that AAPA is being cited as the "prior art". The rejection is respectfully traversed.

Claims 3 to 7 depend from claim 1 and therefore define patentably over AAPA for at least the reasons set forth above with reference to claim 1.

In addition, claim 3 further limits claim 1 by requiring that the thickness of the dielectric sheath be 2.5 microns, minimum on each surface. No such limitation is taught or suggested by AAPA either alone or in the combination as claimed.

Claim 4 further limits claim 1 by requiring that the effective dielectric constant of the sheath surrounding bond wires be in the range of 1.0 to 2.3. No such limitation is taught or suggested by AAPA either alone or in the combination as claimed.

Claim 5 further limits claim 1 by requiring that the distance between wires be in the range of 50 to 100 microns. No such limitation is taught or suggested by AAPA either alone or in the combination as claimed.

Claim 6 further limits claim 1 by requiring that the dielectric constant of the molding compound be in the range of 3.8 to 4.2. No such limitation is taught or suggested by AAPA in the combination as claimed.

Claim 7 further limits claim 1 by requiring that the mutual capacitance between bond wires be lower by a factor of 3 as compared to a device wherein the medium

separating wires has a dielectric constant of 4.0. No such limitation is taught or suggested by AAPA either alone or in the combination as claimed.

Claims 10 and 11 were rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Choi (U.S. 6,013,109). The rejection is respectfully traversed.

Claims 10 and 11 depend from claim1 and therefore define patentably over the applied prior art since Choi fails to overcome the deficiencies in AAPA as indicated above.

In addition, claim 10 further limits claim 1 by requiring that the device be packaged in a Ball Grid Array package. No such limitation is taught or suggested by AAPA in the combination as claimed.

Claim 11 further limits claim 1 by requiring that the device be packaged as a leaded surface mount package. No such limitation is taught or suggested by AAPA in the combination as claimed.

Claim 12 was rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Kim (U.S. 5,801,074). The rejection is respectfully traversed.

Claim 12 requires, among other features, a relatively low dielectric constant sheath surrounding each wire. No such structure is taught or suggested by AAPA, Kim or any proper combination of these references.

Claim 12 further requires a semiconductor package having leads, a substrate, and a housing shell surrounding an open cavity, said relatively low dielectric constant sheath being disposed within the cavity. No such structure is taught or suggested by AAPA, Kim or any proper combination of these references.

Claim 13 has been amended to over come the double patenting rejection.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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